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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,608	03/15/2004	Joseph A. Iadanza	BUR920030174US1	2607

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,608	IADANZA ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,8,12,13,15,19 and 20* is/are rejected.

7)☒ Claim(s) *2-4,7,9-11,14,16-18 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/15/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/708,608 filed on 03/15/2004. Claims 1 –21 remain pending in the application.

Claim Objections

2. Claims are objected to because of the following informalities:

Claim 6, line 7, before "interpolated" insert —**said**—.
Claim 6, line 10, before "characterized" insert —**said**—.
Claim 7, line 3, after "layout" insert —**framework**—.
Claim 7, line 6, change "parasitic netlist" insert —**netlist parasitic extraction**—.
Claim 13, line 7, before "interpolated" insert —**said**—.
Claim 13, line 10, before "characterized" insert —**said**—.
Claim 14, line 3, after "layout" insert —**framework**—.
Claim 14, line 6, change "parasitic netlist" insert —**netlist parasitic extraction**—

Claim 20, line 8, before "interpolated" insert —**said**—.
Claim 20, line 11, before "characterized" insert —**said**—.
Claim 21, line 4, after "layout" insert —**framework**—.
Claim 21, line 7, change "parasitic netlist" insert —**netlist parasitic extraction**—

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 5, 6, 8, 12, 13, 15, 19 and 20 are rejected under 35 U.S.C. 102(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0044510 A1 to *Zolotov et al.*

5. As to Claim 1, *Zolotov et al.* show and teach the following subject matter:

- A method of analyzing circuits using simulation – [title; Paragraph 0001, 0002, 0039 – 0040];
- Creating (a set of) *transistor (table) models* for a circuit has similar *transistors* that different only in their widths using *linear interpolation* of results obtained utilizing previously existing simulations/models ... *fast transistor models* – [Paragraph 0039; Fig. 7]; Notice that (1) *a set of fast transistor models is obtained using models of linear interpolation; it is a set of interpolated models for transistors* (2) linear interpolation models applied to transistors whose functions are linear with sizes (e.g., widths);
- Building (i.e., creating) (a set of) *transistor characterization models* (i.e., *characterized models*) ... each transistor (characterization) model corresponds to a transistor with a unique combination of all its *electrical and geometrical parameters* ... *accurate transistor model* – [Paragraph 0039; Fig. 7]; Notice that a *transistor characterization model* is an *accurate transistor model*;
- Circuit netlist ... transistors...database of transistors models indexed with parameters...(analyzing transistors in a netlist), based on transistor (electrical and geometrical) parameters, to selects *best transistor model* (i.e., *characterized model*) in database that models each transistor in the circuit netlist – [Paragraph 0037; Fig. 7];

Notice that, in designing a circuit, if transistors match *transistor characterization models* (*accurate transistor models*) in a database, the matched characterization models are chosen; otherwise one of interpolated models, which appropriately model each transistor in the netlist, is chosen.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claims 8 and 15, reasons are included in **[Response A]** given above. Notice that transistor characterization model (accurate transistor model) is a direct fit model.

7. As to Claims 5, 12 and 19, in addition to reasons included in **[Response A]** given above, *Zolotov et al.* teach that (1) the linear interpolation models use existing simulation models utilized in the transistor characterization models (actual transistor models) (2) transistor in each actual transistor model is characterized by its electrical and geometrical parameters (i.e., environmental conditions) – [Paragraph 0039]. Therefore the linear interpolation models and transistor characterization models comprise parallel sets of models to characterize transistor sizes and parameters including electrical and environmental conditions.

8. As to Claim 6, in addition to reasons included in **[Response A]** given above, *Zolotov et al.* teach the following subject matter:

- Since transistor models stored in database are indexed, transistors in the circuit netlist which my be simulated with *transistor characterization models* (characterized models) can be recognized – **[Response A**, Paragraph 0039]; Notice that, based on index scheme, (feedback) information relating to which transistors use transistor characterization models can be provided;
- *Linear interpolation modes* provide ***accurate*** and ***fast*** simulation results for transistors whose functions are linear with their sizes – **[Response A**; Paragraph 0039]; Due to utilization existing simulation models, the linear interpolation modes would benefit from the characterized models – [Response A; Paragraph 0039]. Notice that a circuit netlist can be analyzed to determine transistors whose functions are linear with their size to apply the linear interpolation models.

It is well known in the art that *linear interpolation models* will not provide accurate simulation results when functions of transistors are nonlinear with their sizes. In order to achieve accurate results and to facilitate switching to existing characterized models, changes to circuit netlist that contain those nonlinear transistors should be simulated. Notice that those changes require back annotating (i.e., modifying) a series of scenarios to (original) circuit design layout framework of transistors in the netlist for designer selection.

For reference purposes, the explanations given above in response to Claim 6 are called **[Response B]** hereinafter.

9. As to Claims 13 and 20, reasons are included in **[Response B]** given above. Notice that transistor characterization model (accurate transistor model) is a direct fit model.

Allowable Subject Matter

10. Claims 2 – 4, 7, 9 – 11, 14, 16 – 18 and 21 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A method of analyzing/designing (electrical) circuits comprises *schematically simulation a custom circuit*, *extracting saturation and dynamic linear mode transistors*, *back annotating a netlist of the customer circuit to a schematic with a predetermined device state* and *performing sensitivity analysis on saturation and dynamic linear mode transistors* in combination with other limitations as recited in **Claim 2** and **Claim 9**, respectively;
- A program storage device embodying a computer program to perform a method of analyzing/designing (electrical) circuits comprises *schematically simulation a custom circuit*, *extracting saturation and dynamic linear mode transistors*, *back annotating a netlist of the customer circuit to a schematic with a predetermined device state* and *performing sensitivity analysis on saturation and dynamic linear mode transistors* in combination with other limitations as recited in **Claim 16**;
- A method of analyzing/designing (electrical) circuits comprises *selecting propagated information tags in netlist parasitic extraction* and *simulating the netlist parasitic extraction to ensure post-layout integrity* in combination with other limitations as recited in **Claim 7** and **Claim 14**, respectively;
- A program storage device embodying a computer program to perform a method of analyzing/designing (electrical) circuits comprises *selecting propagated information tags in netlist parasitic extraction* and *simulating the*

netlist parasitic extraction to ensure post-layout integrity in combination with other limitations as recited in **Claim 21**.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
November 21, 2005